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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
RICHARDS, N DREW	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 09/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	Application No.	Applicant(s)
	10/067,424	LU ET AL.
	Examiner	Art Unit
	N. Drew Richards	2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *7-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 7-19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 7, 11 and 16 all contain the limitation of the second passivation layer suppressing lateral leakage current between collection electrodes. This limitation is indefinite as the claims do not define what level of current the lateral leakage is being reduced from or what level of current occurs after the lateral leakage has been reduced. Suppressing a feature, in this case lateral leakage current, is indefinite when no definite point of comparison has been defined in the claims. The relative terminology is indefinite since one would not be reasonably ascertained of what level of leakage reads on the "suppress"ed leakage. Claims 8-10, 12-15 and 17-19 are similarly rejected as they do not correct the deficiencies of the claims from which they depend.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 7 – 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art (AAPA) in view of Ishaque et al. (USPAT 5288989, Ishaque) and Possin et al. (USPAT 5777355, Possin).

With regard to claim 7, the AAPA discloses in figure 2 a method for making a high fill factor image array (40). The AAPA discloses in figure 2 providing a plurality of source-drain metal contacts (44) on a substrate (42). The AAPA discloses in figure 2 depositing a first passivation layer (first three quarters of the thickness of 56 deposited on 42) over the plurality of source-drain metal contacts and the substrate. The AAPA discloses on page 2, lines 19 – 20 that a preferred material for the first passivation layer is silicon oxynitride. The AAPA also discloses on page 3, lines 11 – 18 that an interface with the silicon oxynitride and an overlying layer causes conducting channels to occur between two lateral pixel electrodes. The AAPA further discloses on page 3, lines 19 – 21 a material different than silicon oxy-nitride as a first passivation layer is advantageous to prevent the conducting channels from forming between two pixel electrodes. The AAPA does not discuss using a particular different passivation layer. Ishaque teaches in figure 1 depositing a passivation layer that comprises depositing a first passivation layer (132) over underlying devices and depositing a second passivation layer (134) over the first passivation layer. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the dual passivation layer of Ishaque in the method of the AAPA in order to use a passivation layer that reduces capacitive coupling between device structures as is known in the art, reduces leakage, and provides a moisture barrier to the improved passivation layer as

taught by Ishaque in column 7, lines 21 - 42. Further, any processing occurring after the deposition of the first passivation layer in the AAPA will now occur after the deposition of the first and second passivation layers of Ishaque. The AAPA discloses in figure 2 (taken together with the teaching of Ishaque) opening a plurality of via holes through the first and second passivation layers to the plurality of source-drain metal contacts. The AAPA discloses in figure 2 (taken together with the teaching of Ishaque) depositing a layer of conductive material (layer above arrow pointing out 46) over the plurality of source-drain metal contacts and the second passivation layer. The AAPA discloses in figure 2 depositing a first doped a-Si layer (48) over the layer of conductive material. The AAPA discloses in figure 2 patterning the first doped a-Si layer and the layer of conductive material to form the collection electrodes (46). The AAPA discloses in figure 2 (taken together with the teaching of Ishaque) depositing a continuous layer of i a-Si (50) disposed on the second passivation layer and the first doped a-Si layer. The AAPA discloses in figure 2 depositing a continuous second layer of doped a-Si (52) over the continuous layer of i a-Si. The AAPA discloses in figure 2 depositing an upper conductive layer (54) over the second layer of doped a-Si. It is not clear if the AAPA and Ishaque teach patterning the upper conductive layer to form the image array. Possin teaches in figures 1 and 2; and in the abstract depositing and patterning an upper conductive layer (28). It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the patterning step of Possin in the method of the AAPA and Ishaque in order to differentiate the device into a plurality of devices, thus creating an array, which results in cost savings over having to make a

plurality of devices separately. It would have been further obvious in the method of the AAPA in view of Ishaque and Possin that the patterning would form an image array. In using the dual passivation layer of Ishaque in the method of the AAPA, the second passivation layer suppresses leakage current between the collection electrodes.

With regard to claim 11, the AAPA discloses in figure 2 a high fill factor image array (40) forming process. The AAPA discloses in figure 2 providing a plurality of source-drain metal contacts (44) on a substrate. The AAPA discloses in figure 2 depositing a first passivation layer (first three quarters of the thickness of 56 deposited on 42) over the plurality of source-drain metal contacts and the substrate (42). The AAPA discloses on page 2, lines 19 – 20 that a preferred material for the first passivation layer is silicon oxynitride. The AAPA also discloses on page 3, lines 11 – 18 that an interface with the silicon oxynitride and an overlying layer causes conducting channels to occur between two lateral pixel electrodes. The AAPA further discloses on page 3, lines 19 – 21 a material different than silicon oxy-nitride as a first passivation layer is advantageous to prevent the conducting channels from forming between two pixel electrodes. The AAPA does not discuss using a particular different passivation layer. Ishaque teaches in figure 1 depositing a passivation layer that comprises depositing a first passivation layer (132) over underlying devices and depositing a second passivation layer (134) over the first passivation layer. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the dual passivation layer of Ishaque in the method of the AAPA in order to use a passivation layer that reduces capacitive coupling between device structures as is

known in the art, reduces leakage and provides a moisture barrier to the improved passivation layer as taught by Ishaque in column 7, lines 21 - 42. Further, any processing occurring after the deposition of the first passivation layer in the AAPA will now occur after the deposition of the first and second passivation layers of Ishaque. The AAPA discloses in figure 2 (taken together with the teaching of Ishaque) opening a plurality of via holes through the first and second passivation layers over the plurality of source-drain metal contacts. The AAPA discloses in figure 2 (taken together with the teaching of Ishaque) depositing a layer of conductive material (layer above arrow pointing out 46) on the plurality of source-drain metal contacts and over the second passivation layer. The AAPA discloses in figure 2 depositing a first doped a-Si layer (48) over the layer of conductive material. The AAPA discloses in figure 2 patterning the first doped a-Si layer and the layer of conductive material to form the collection electrodes (46). The AAPA discloses in figure 2 (taken together with the teaching of Ishaque) depositing a continuous layer of i a-Si (50) disposed on the second passivation layer and over the first doped a-Si layer. The AAPA discloses in figure 2 depositing a continuous second layer of doped a-Si (52) over the continuous layer of i a-Si. The AAPA discloses in figure 2 depositing an upper conductive layer (54) over the continuous second layer of doped a-Si. It is not clear if the AAPA and Ishaque teach patterning the upper conductive layer. Possin teaches in figures 1 and 2; and in the abstract depositing and patterning an upper conductive layer (28). It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the patterning step of Possin in the method of the AAPA and Ishaque in order to

differentiate the device into a plurality of devices, thus creating an array, which results in cost savings over having to make a plurality of devices separately. It would have been further obvious in the method of the AAPA in view of Ishaque and Possin that the patterning would form an image array. In using the dual passivation layer of Ishaque in the method of the AAPA, the second passivation layer suppresses leakage current between the collection electrodes.

With regard to claim 16, the AAPA discloses in figure 2 a method for making a high fill factor image array (40). The AAPA discloses in figure 2 providing a plurality of source-drain metal contacts (44). The AAPA discloses in figure 2 depositing a first passivation layer (first three quarters of the thickness of 56 deposited on 42) over the source-drain metal contact. The AAPA discloses on page 2, lines 19 – 20 that a preferred material for the first passivation layer is silicon oxy-nitride. The AAPA also discloses on page 3, lines 11 – 18 that an interface with the silicon oxy-nitride and an overlying layer causes conducting channels to occur between two lateral pixel electrodes. The AAPA further discloses on page 3, lines 19 – 21 a material different than silicon oxy-nitride as a first passivation layer is advantageous to prevent the conducting channels from forming between two pixel electrodes. The AAPA does not discuss using a particular different passivation layer. Ishaque teaches in figure 1 depositing a passivation layer that comprises depositing a first passivation layer (132) over underlying devices and depositing a second passivation layer (134) over the first passivation layer. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the dual passivation layer of Ishaque in the method

of the AAPA in order to use a passivation layer that reduces capacitive coupling between device structures as is known in the art, reduces leakage and provides a moisture barrier to the improved passivation layer as taught by Ishaque in column 7, lines 21 - 42. Further, any processing occurring after the deposition of the first passivation layer in the AAPA will now occur after the deposition of the first and second passivation layers of Ishaque. The AAPA discloses in figure 2 (taken together with the teaching of Ishaque) opening a via hole through the first and second passivation layers to expose the source-drain metal contact. The AAPA discloses in figure 2 depositing a layer of conductive material (46) on the source-drain metal contact, such that the layer of conductive material makes electrical contact with the source-drain metal contact. The AAPA discloses in figure 2 depositing a first doped a-Si layer (48) on the layer of conductive material. The AAPA discloses in figure 2 patterning the a-Si layer and the layer of conductive material to form a collection electrode (46). The AAPA discloses in figure 2 (taken together with the teaching of Ishaque) depositing sensor material comprising a continuous layer of i a-Si (50) over the collection electrode and at least a portion of the second passivation layer. The AAPA discloses in figure 2 depositing a continuous layer of doped a-Si (52) over the continuous layer of i a-Si. The AAPA discloses in figure 2 depositing a conductive layer (54) over the continuous layer of doped a-Si. The AAPA discloses in figure 2 that the conductive layer is an upper electrode. It is not clear if the AAPA teaches patterning the upper conductive layer to form the upper electrode. Possin teaches in figures 1 and 2; and in the abstract depositing and patterning a conductive layer (28) to form an upper electrode. It would

have been obvious to one of ordinary skill in the art at the time of the present invention to use the patterning step of Possin in the method of the AAPA in order to differentiate the device into a plurality of devices, thus creating an array, which results in cost savings over having to make a plurality of devices separately. In using the dual passivation layer of Ishaque in the method of the AAPA, the second passivation layer suppresses leakage current between the collection electrodes.

With regard to claims 8, 12, and 17, the Ishaque teaches in figure 1 and column 5, lines 15 – 29 wherein the first passivation layer comprises BCB.

With regard to claims 9, 13, and 18, Ishaque teaches in figure 1 and the abstract wherein the second passivation layer is an oxide.

With regard to claim 10, 14, and 19, Ishaque teaches in figure 1, column 5, lines 25 – 27 and 52 – 53 wherein the thickness of the second passivation layer is less than the thickness of the first passivation layer.

With regard to claim 15, Ishaque teaches in figure 1 and column 5, 52 – 53 wherein the second passivation layer has a thickness of about 1000 Å (i.e. the range of between about 400 Å and 1 micron encompasses the claimed range of about 1000 Å).

Response to Arguments

5. Applicant's arguments filed July 1, 2005 have been fully considered but they are not persuasive.

Applicant has argued that the combination of Ishaque et al. and the AAPA does not teach deposition of a second passivation layer in AAPA because there would be no motivation for one skilled in the art to place a barrier layer into Applicant's high fill factor array structure. Applicant furthers this argument by stating that the structures taught by applicant and the structure taught by Ishaque et al. are widely different and the passivation layers have largely different purposes and effects. First, various motivations are given in Ishaque et al. that would suggest placing their two-tier passivation layer in the structure of the AAPA. For instance, Ishaque et al. teach that their two-tier passivation layer provides 1) an electrically insulating barrier, 2) the ability to cover the underlying structure without cracking or inducing stresses that adversely effect the dielectric integrity of the passivating layer, 3) an interface with the passivating layer that has minimal conductivity so that leakage in reverse bias is not degraded, 4) a layer thick enough so that the electric field inside the dielectric layer does not become very large, and 5) protection from degradation due to humidity, moisture, or chemical attack from materials in the environment or present on the wafer during fabrication and over time as the device is exposed to a variety of environments. See Ishaque et al. column 2 lines 3-31. Ishaque et al. teaches drawbacks of using a single passivation layer and overcomes these drawbacks and obtains a passivation layer with the desirable characteristics outlined above by providing their two-tier passivation layer. Thus, for all the reasons 1-5 above, one would be motivated to use the two-tier passivation layer of Ishaque et al. in the structure of the AAPA. Further, the differences in structure between the AAPA and Ishaque et al. in no way teach against using the two-tier

passivation layer in the AAPA. The AAPA recognizes the need for a passivation layer and uses it as insulation between conductors. The AAPA then recognizes that leakage occurs at the interface with the passivation layer. The AAPA then also recognizes that using silicon oxide as the passivation layer is one solution but that the deposition rate is slow and stress build-up may degrade the structure. Since Ishaque et al. directly discusses passivation layers desirably acting as an electrically insulating barrier, having minimal conductivity at the interface, and not inducing cracking or stress, it is clear that the two-tier passivation layer of Ishaque et al. has the same purpose and effect as the passivation layer in the AAPA as well as overcoming the deficiencies recognized in the passivation layer of the AAPA. Thus, the combination of references do teach the claimed limitations and the combination is proper.

Applicant has further argued that the motivation for combining the references as previously explained, specifically reducing capacitive coupling, is already performed by the AAPA and thus the AAPA does not need the addition of a second passivation layer to fulfill this function. This is not persuasive. First, the passivation layer of the AAPA has been shown in applicant's background section to be defective. As such, a need is recognized for better passivation, this is provided by the two-tier passivation layer of Ishaque et al. Thus, proper motivation does exist for the combination. As to the previously stated motivation of reducing capacitive coupling. One of ordinary skill in the art would recognize that the use of lower dielectric constant materials for the passivation layer (i.e. the organic layer and silicon oxide of Ishaque et al.) would inherently reduce capacitive coupling compared to using the silicon nitride passivation layer of the AAPA.

It is well known in the art that silicon oxide and organics (such as the polyimide taught by Ishaque et al.) have a lower dielectric constant than silicon oxynitride. Though not explicitly stated in the references, this is still considered a valid motivation as it is well known to reduce capacitive coupling to reduce RC delay and crosstalk and noise between various components.

Applicant also argues that a layer that does not cover a significant portion of the device does not make a moisture barrier and there is no need of a moisture barrier at a point where the barrier layers are fully encapsulated in the device. This is not persuasive. First, the area covered by the passivation layer (and thus the area protected against moisture) does not need to be a large portion of the device, protecting even a small area from moisture will still offer an improvement over not protecting any area. Second, a moisture barrier is still needed at a point where the barrier layers are fully encapsulated in the device because moisture is a concern not only in the final encapsulated device, but also during fabrication and the source of the moisture can be not only the atmosphere or environment the device operates in, but can come from previously formed layers or from the deposition chemistries used to deposit layers. As such, a moisture barrier is useful during the fabrication process over any portion of the device.

Applicant also argues in response to the Examiner's previous response to arguments that the Examiner does not deny that Ishaque teaches away from the use of amorphous silicon in the structure and that the Examiner's argument reveals how different the structure taught in Ishaque is from the structure taught from AAPA and

further provides evidence that there would be no motivation to combine the AAPA with Ishaque. First, though Ishaque may preferably use a material other than amorphous silicon, Ishaque does not provide any explicit teaching that using the amorphous silicon of the AAPA in the device of the AAPA is detrimental. Second, it is not clear how the Examiner's previous response reveals now different the structure taught in Ishaque is from the structure taught in the AAPA. It is readily recognized that there are differences in the structures of the two references, but this has no bearing on whether one of ordinary skill in the art would be motivated to combine the references in the manner proposed in the rejections above. In this case, they are similar devices, from the same field of endeavor, that both use passivation layers and have concerns with their passivation layers. Since Ishaque et al. clearly provides an improved passivation layer one of ordinary skill in the art would recognize the desirability of making the combination.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to N. Drew Richards whose telephone number is (571) 272-1736. The examiner can normally be reached on Monday-Friday 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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